24. (Once Amended) The computer readable medium as set forth in claim 23, wherein instructions for determining a new drive current for said circuit from said drive voltage and said load capacitance comprises instructions for:

storing a circuit characterization model for said circuit, said circuit characterization model depicting relationships among input signal slew rate, load capacitance, drive current and drive voltage for said circuit; and

selecting an input signal slew rate for simulation of an input signal to said circuit; and

accessing said circuit characterization model to extract a drive current based on said drive voltage, effective capacitance, and said input signal slew rate selected.

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

Overview of the Claimed Invention:

A variable current source model accurately determines timing delays for integrated circuit designs. The design specifies a resistive-capacitive ("RC") network that couples a driving point and a receiving point. A circuit specified in the design, such as a gate level circuit implemented in a standard cell, drives the RC network at the driving point. The variable current source model determines driving currents for the circuit at the driving point based on the RC network and a characterization of the circuit. Specifically,

time instances, which correspond to output voltages of the circuit, are specified. A load capacitance for the circuit is dynamically determined. In one embodiment, the load capacitance is determined from the charging and discharging of the RC network from the drive current. For each time instance, a new drive current for the circuit is determined from the drive voltage and the load capacitance from the previous time instance. A receiving voltage for each time instance is determined from the drive voltage and a transfer function for the RC network.

Rejection of the Claims Under 35 U.S.C. § 103

In the Office Action dated January 24, 2003, claims 1, 5, 8, 10, 13, 17 and 22 were rejected under 35 U.S.C. § 103 as being obvious over US Patent 6,314,546, issued to Muddu (hereafter referred to as "*Muddu*"). The Examiner objected to the Specification for an informality. Also, claims 10, 22 and 24 were objected to for some informalities. Claims 2-4, 6-7, 9, 11, 12, 14, 16, 18-21 and 23-24 were objected to as being dependent upon a rejected claims, but would be allowable if rewritten in independent form including all of the base claim and any intervening claims. Claim 25 was allowed.

A. *Muddu* Does Not Disclose Determining Timing Delay Parameters From Effective Driving Currents.

Claim 1 recites, in part:

determining a plurality of effective driving currents for said circuit at said driving point based on said circuit characterization model; and

determining timing delay parameters from said effective driving currents.

Claims 10, 13 and 22 include similar limitations.

The Examiner noted that *Muddu* does not explicitly teach determining a plurality of effective driving currents. (01/24/03 Office Action, page 4). However, in concluding that *Muddu* renders claims 1, 8 and 13 obvious, the Examiner argued that since the effective capacitance is determined in the range between the step input capacitance C_{set} and the total capacitance C_{tot} under full load conditions, and the gate response is depending on charging of capacitance load, it would have been obvious to one of ordinary skill in the art to determine a plurality of effective driving currents to determine timing delays. Applicants respectfully contend that *Muddu* does not render the claimed invention obvious because *Muddu* does <u>not</u> teach or suggest the advantage of using effective driving currents to determine timing delay parameters.

B. The Use of Effective Driving Currents To Determine Timing Delay Parameters More Accurately Models Circuit Behavior.

The step of calculating effective driving currents accurately determines load capacitance from the charging and discharging of the RC network from the drive current. This approach, referred to in the Specification as the variable current source, models the

true behavior of the circuit under analysis by considering the non-linear voltage-current characteristics of the circuit. Applicants disclose, in the Specification:

> As illustrated in the example of Figures 3A-C, the iterative technique of calculating current based on the voltage, and thus the changing capacitance, at multiple time instances for a circuit under analysis may be modeled as a variable current source. The variable current source of the present invention accounts for the true behavior of a driver circuit under analysis by considering the non-linear voltage-current (V-I) characteristics of the switching transistors of the circuit. Thus, the variable current source technique accurately captures the resistive shielding of the RC network. (Specification, page 11, line 6 – 12).

Thus, the claimed invention tracks the resistive shielding of the RC network by using the effective driving currents. Accordingly, it would not have been obvious to modify *Muddu* to determine timing parameters from the effective drive currents because *Muddu* does not disclose or suggest an approach that accounts for the non-linear V-I characteristics of a circuit under analysis, as claimed.

CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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The Amended Claims

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined to show the changes made.

10. (Once Amended) A method for characterizing a circuit for determining a timing delay, said method comprising the step of:

determining a resistive-capacitive ("RC") network between a driving point and a receiving point, said circuit driving said RC network at said driving point;

selecting a plurality of time instances for analysis of said circuit;

determining a load capacitance for each of said time instances, said load capacitance specifying a capacitance from said driving point of said circuit;

determining operation of said circuit at a new time instance based on said load capacitance of a previous time instance; and

determining timing delay parameters based on [operation of said circuit and] a response to said RC network at said time instances.

22. (Once Amended) A computer readable medium, comprising a plurality of instructions, which when executed by a computer, causes the computer to determine timing delays for a circuit in an integrated circuit, said instructions for:

determining a resistive-capacitive ("RC") network between a driving point and a receiving point, said circuit driving said RC network at said driving point;

selecting a plurality of time instances for analysis of said circuit;

determining a load capacitance for each of said time instances, said load capacitance specifying a capacitance from said driving point of said circuit;

determining operation of said circuit at a new time instance based on said load capacitance of a previous time instance; and

determining timing delay parameters based on [operation of said circuit and] a response to said RC network at said time instances.

24. (Once Amended) The computer readable medium as set forth in claim [22] 23, wherein instructions for determining a new drive current for said circuit from said drive voltage and said load capacitance comprises instructions for:

storing a circuit characterization model for said circuit, said circuit characterization model depicting relationships among input signal slew rate, load capacitance, drive current and drive voltage for said circuit; and

selecting an input signal slew rate for simulation of an input signal to said circuit; and

accessing said circuit characterization model to extract a drive current based on said drive voltage, effective capacitance, and said input signal slew rate selected.

The Amended Specification

In response to the Office Action dated January 24, 2003, please amend the patent application as follows:

The voltage signals input to a circuit are characterized by input signal slew rate. In general, the input signal slew rate measures the rate at which the voltage rises from 10% of V_{dd} to 90% of V_{dd} or falls from 90% of V_{dd} to 10% of V_{dd}. For the example in Figure 1, the driving instance delay is the time delay exhibited by driver 110 to propagate a signal as measured by the time difference required to generate a voltage, V_d, at the output of driver 110 from an input voltage in input vector 105. The gate level circuit (*e.g.*, driver 110) may include one or more inputs. The input vectors represent the combinations of different inputs states. The example of Figure 1 has only one input signal that transitions from 0 to 1 or from 1 to 0, thereby causing the output signal to switch from 1 to 0 or 0 to 1, respectively. For the simplified driver circuit of Figure 1, which includes only one input, input vectors 105 include one input waveform that transitions from a low logic level to a high logic level, and a second input vector that transitions from a high logic level to a low logic level. As described below in conjunction with Figure 2, the circuit may include multiple inputs, and the input vectors may include different combinations of signal transitions for the multiple inputs.